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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,552	03/30/2005	Tatsuya Kamei	XA-10260	9339
181 7590 10/17/2007 MILES & STOCKBRIDGE PC 1751 PINNACLE DRIVE SUITE 500 MCLEAN, VA 22102-3833			EXAMINER NGUYEN, THAN VINH	
			ART UNIT 2187	PAPER NUMBER
			NOTIFICATION DATE 10/17/2007	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipdocketing@milesstockbridge.com
sstiles@milesstockbridge.com

Office Action Summary

Application No.

10/521,552

Applicant(s)

KAMEI ET AL.

Examiner

Than Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 August 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 5-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 5-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 January 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This is a response to the amendment, filed 8/10/07.
2. Claims 2-4 and 16-20 have been canceled. Claims 1 and 5-15 remain pending.
3. The IDS, filed 6/7/05, has been considered.

Response to amendment

4. In view of the amendment to the title, the previous objection to the title is withdrawn.
5. In response to the cancellation of claims 2-3, the previous rejection to these claims under 35 USC 112, is moot.
6. The amended claims are addressed below. Applicant's amendment introduces vagueness into the claim language. See 35 USC 112 rejection below.

Claim Rejections - 35 USC § 112

7. Claims 1,5-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. As to claim 1, Applicant added the limitation of:

“a complementary transfer source address or transfer destination address of the block transfer is a physical address corresponding to a different logical address, and is associated with a second transfer object”.

It is unclear as what is being claimed in the above limitation. Is Applicant claiming an address (complementary transfer source/transfer destination address”? It is not clear how the above address relates to the rest of the claimed limitations and how it is used in the invention. Applicant must also point out the location of the support of the above limitation in the

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specification since the term “complementary transfer source address” is not defined in the specification. Clarification of the claim language is required. For examination purposes, the Examiner will interpret the above language to mean that a different transfer object has a different logical address.

8. Claims 5-15 are also rejected for incorporating the error of the parent claim.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-9,14,15 are rejected under 35 U.S.C. 102(e) as being anticipated by Nagayasu (US 6,801,988).

As to claim 1:

11. Nagayasu teaches a data processor comprising: a CPU (CPU 1); a cache (cache 4); an internal memory accessible by said CPU (SDRAM 3); and a control circuit (memory controller 2) capable of responding to a particular access request issued by said CPU to control a block transfer, in which said internal memory is used as one transfer object, wherein a set of instructions for said CPU includes a particular instruction for making said CPU issue the particular access request (transfer command 2/50-57; 4/19), the particular instruction has an addressing field, and when an address specified by the addressing field coincides with an

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address mapped to said internal memory, the address is set as one of transfer source and transfer destination addresses of the block transfer (destination address of data transfer; 2/20-33). A different transfer object/block would correspond to a different logical address (each destination address corresponds to a different encoded address; 2/25-30,59-63).

As to claim 5,14,15:

12. Nagayasu teaches a bus interface controller connected to said control circuit, wherein said bus interface controller is capable of performing interface control of the other transfer object (address/data bus CADD/CDATA; Fig. 1).

As to claim 6:

13. Nagayasu teaches a cache memory, wherein said cache memory shares a first bus with said CPU, internal memory, and control circuit (cache 4; 4/25-35).

As to claim 7:

14. Nagayasu teaches wherein said internal memory is assigned a cache non-object address for said cache memory (cache address different from SDRAM address; 4/40-44).

As to claim 8:

15. Nagayasu teaches a second bus used exclusively for connecting said control circuit with said internal memory, wherein said second bus can be utilized for data block transfer in response to the particular access request (MDATA, MADD, MDS buses; 4/25-35).

As to claim 9:

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16. Nagayasu teaches control circuit is capable of performing memory control in regard to a cache hit and cache miss with respect to said cache memory (4/36-44).

Allowable Subject Matter

17. Claims 10-13 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

18. As to claim 10, the prior art does not further teach wherein the particular instruction includes a first cache memory-operating instruction, and when the logical address specified by the addressing field directs a cache object address for said cache memory, the first cache memory-operating instruction causes an operation of making said cache memory retain data of an external memory associated with the physical address corresponding to the different logical address, at a cache object address specified by the logical address.

19. Claims 11-13 are also allowable for incorporating the limitations of claim 10, and further limitations.

Conclusion

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after


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the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is 571-272-4198. The examiner can normally be reached on 8am-3pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


Than Nguyen
Primary Examiner
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